CLAIMS

1. An apparatus comprising:

a memory configured to (i) read and/or write a plurality of state vectors and (ii) read and/or write data;

an encoder configured to present state vectors to be written in response to (i) data read from said memory, (ii) a first address and (iii) a serial data stream; and

one or more registers configured to present said first address in response to an input address.

2. The apparatus according to claim 1, further comprising a counter circuit configured to generate said input address.

3. The apparatus according to claim 1, further comprising an address register configured to store said first address and present a second address.

4. The apparatus according to claim 2, wherein said encoder further comprises:

a state machine configured to (i) a monitor for one or more pattern match conditions, (ii) continue to monitor said serial stream for both valid and invalid pattern match conditions, and (iii) continue to monitor for said pattern match conditions and implement a count bit field to track said pattern match conditions and one or more non-match conditions;

a compare circuit configured to (i) control said state machine and (ii) compare said register address and said second address; and

a gate configured to control said state machine in response to a bit of said data read and said serial data stream.

5. The apparatus according to claim 4, wherein said state machine comprises:

a first logic section configured to increase a value representing the number of sequential bits found that match a framing pattern; and

a second logic section configured to determine if an incrementer is tracking one or more framing sequence matches or mismatches, and if framing has been validated.

6. The apparatus according to claim 4, wherein said state machine is configured to simultaneously validate framing at all possible locations in a serial stream.

7. The apparatus according to claim 5, wherein said apparatus may retain said framing in the presence of bit errors and provide a reframe condition following a loss of framing that occurs in less than two frames.

8. The apparatus according to claim 7, wherein said apparatus is further configured to postpone indication of valid framing until a single framing match is present.

9. The apparatus according to claim 8, wherein said apparatus is further configured to frame within approximately NxI bits, where N is an integer representing a number of bits required to indicate detection of a valid framing sequence and I is an integer representing an interleave depth.

10. The apparatus according to claim 9, wherein said apparatus is configured to (i) detect one or more bit-offset

locations meeting the requirements of the framing sequence, and (ii) withhold completion of framing until said bit offset locations resolve to a single offset location.

11. The apparatus according to claim 1, wherein said memory comprises a synchronous DPRAM.

12. The apparatus according to claim 1, wherein said memory comprises a SRAM with read-modify-write access.

13. The apparatus according to claim 1, wherein said memory comprises two banks of standard RAM, wherein a first bank is accessed for sequential read operational and a second bank is accessed for sequential write operations.

14. The apparatus according to claim 1, wherein said memory comprises a FIFO having a character depth of at least that of an interleave depth and a character width of at least that of a normal state vector, plus one more bit serving as an interleave boundary marker.

15. A method for detection of framing in a bit interleaved data stream, comprising the steps of:

(A) reading and/or writing a plurality of state vectors;

(B) presenting data to be written in response to (i) data read, (ii) a first address and (iii) a serial data stream; and

(C) presenting said first address in response to an input address.

16. The method according to claim 15, wherein said method simultaneously validates framing at all possible locations in said serial data stream.

17. The method according to claim 15, wherein said method postpones indication of valid framing until a single framing match is present.

18. The method according to claim 15, wherein said method retains framing in the presence of bit errors.

19. The method according to claim 15, wherein said method allows a reframe following loss of framing to occur in less than two frames.

20. An apparatus comprising:

means for storing a plurality of state vectors;

means for presenting state vectors to be written in response to (i) data read, (ii) a first address and (iii) a serial data stream; and

means for presenting said first address in response to an input address.